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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/797,240 | 03/10/2004 | Duc V. Ho | MICS:0120 (03-0231) | 2999 |

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Michael G. Fletcher
Fletcher Yoder
P.O. Box 692289
Houston, TX 77269-2289

| EXAMINER | |
|---|---|
| LE, THONG QUOC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/797,240 | HO ET AL. | |
| | Examiner | Art Unit | |
| | Thong Q. Le | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-43* is/are allowed.

6)☒ Claim(s) *1,2,12,20-25,29 and 30* is/are rejected.

7)☒ Claim(s) *3-11,13-19,26-28,31-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-43 are presented for examination.

### *Information Disclosure Statement*

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 03/10/2004.

3. Information disclosed and list on PTO 1449 was considered.

### *Specification*

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-2, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Silla et al. (U.S. Patent No. 6,552,949).

Regarding claim 1, 12, Silla et al. disclose a system (Figure 1) comprising:

a processor (Figure 1, 10) , and

a memory device (50) coupled to the processor and comprising:

a regulator (70) control coupled to an external voltage source; and

a plurality of internal voltage buses (95) coupled to the regulator control to provide power to a plurality of circuits, wherein at least one of the plurality of internal voltage buses comprises a plurality of control circuitry having at least one level shifter configured to receive at least one disable signal and at least one data signal; provide a determined output signal when the at least one disable signal corresponds to a deep power down mode; and provide an output signal that is based on the at least one data signal when the at least one disable signal does not correspond to the deep power down mode (Column 2, lines 50-67, Column 3, lines 1-15).

Regarding claim 2, Silla et al. disclose wherein the plurality of internal voltage buses comprises an operating voltage bus that provides an operating voltage to output buffer circuitry (Column 8, lines 10-17).

7. Regarding claims 29-30, the apparatus discussed above would perform the method claims 29-30.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 20-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Clark et al (U.S. Patent No. 6,519,707).

Regarding claims 20-25, Clark et al. disclose a memory device (Figure 1) comprises:

a regulator control (120) coupled to an external voltage source;

a voltage bus (160) coupled to the regulator control to provide power to a plurality of circuits (Column 5, lines 5-10),

a control circuitry (125) coupled to the voltage bus having a level shifter that is configured to: receive a disable control signal and a data signal; provide a predetermined output signal when the disable control signal corresponds to a deep power down mode; provide an output signal that is based on the data signal when the disable control signal does not correspond to a deep power down mode (Column 5, lines 25-49,Column 10, lines 1-37), and wherein the memory device comprises a DRAM device (Figure 3, 340), and wherein the memory device comprises a static random access memory (SRAM) device (Column 9, lines 65), and wherein the regulator control comprises a grounding device configured to ground the voltage bus when a deep power down signal is received at the regulator control (Column 10, lines 15-25), and output buffer circuitry (Column 5, lines 25), and delay lock loop (Column 6, lines 1-5).

***Allowable Subject Matter***

9. Claims 3-11, 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-11, 31-33 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Silla et al. (U.S. Patent No. 6,552,949), Clark et al. (U.S. Patent No. 6,519,707), and others, does not teach the claimed invention having a plurality of internal voltage buses comprises an array voltage bus provides an array voltage to array circuitry.

10. Claims 13-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 13-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Silla et al. (U.S. Patent No. 6,552,949), Clark et al. (U.S. Patent No. 6,519,707), and others, does not teach the claimed invention having at least one data signal comprises a first disable and a second disable signal.

11. Claims 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 26-28 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Silla et al. (U.S. Patent No. 6,552,949), Clark et al. (U.S. Patent No. 6,519,707), and others, does not teach the claimed invention having level shifter comprises a first transistor coupled between a first output terminal and a low voltage source, and a second transistor coupled between a second output terminal and the low voltage source.

12. Claims 34-43 are allowed.

Claims 34-43 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Silla et al. (U.S. Patent No. 6,552,949), Clark et al. (U.S. Patent No. 6,519,707), and others, does not teach the claimed invention having a method of providing a deep power down mode, the method comprising receiving at least one disable control signal and a data signal at a level shifter; providing a predetermined output signal when the at least one disable control signal corresponds to a deep power down mode; and providing an output signal based on the data signal when the at least one disable control signal does not correspond to the deep power down mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER